

A cmos photonics based 10Gbps fiber optic communication link

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Abstract

A 10Gbps fiber optic communication link using cmos photonics is analyzed and demonstrated to be feasible as a low cost, low power, highly integrated solution for next generation networks. The optical transceiver uses a 0.13 μ m SOI process to implement an integrated TX and RX module capable of driving greater than 2km of Single Mode (SM) fiber. The optical transceiver core operates at 10Gbps with a BER of less than 10×10^{-15} and a power consumption of 1.25W per channel.

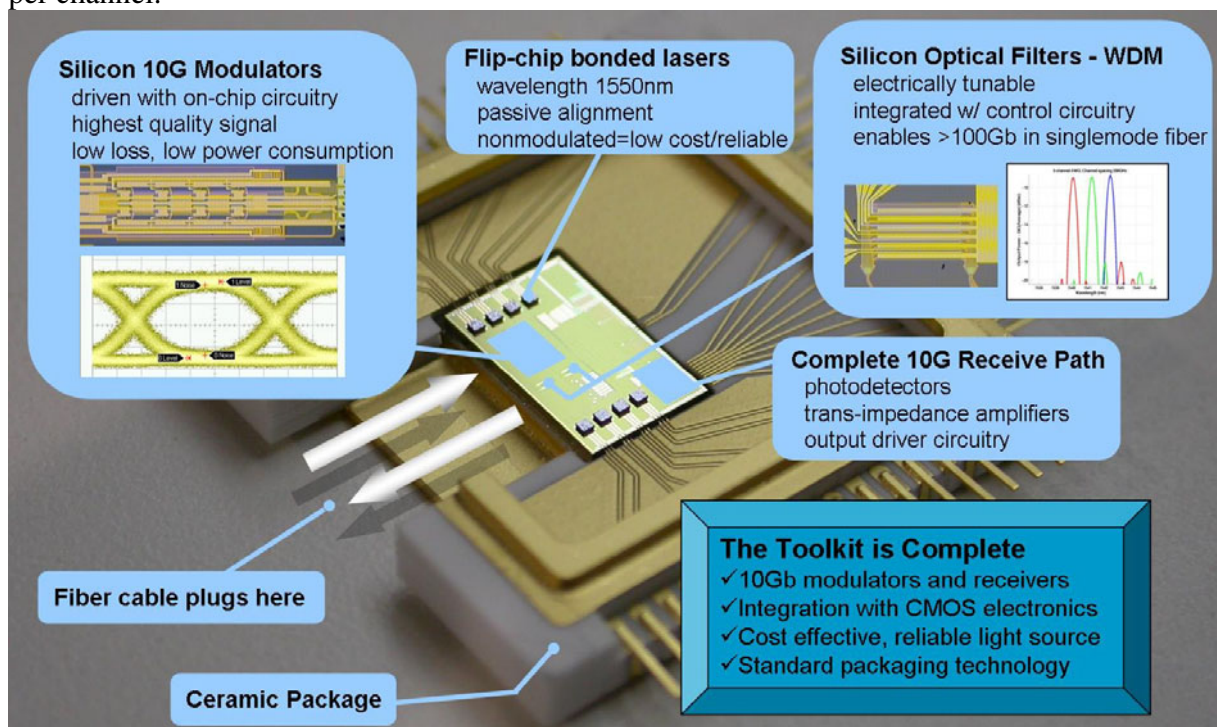


Figure 1. Overview of CMOS Photonics technology

Introduction

As data networks scale to increase throughput, some of the major obstacles that limit serial data rates in copper channels are signal attenuation, dispersion and cross-talk. These problems become more pronounced at higher data rates, drastically limiting the reach of copper links at data rates of 10-Gb/s and above [1]-[2]. The scalability of a single strand of fiber to higher bandwidths through optical techniques such as wavelength division multiplexing (WDM), together with the limited capacity and reach of copper links, suggest that fiber will replace copper even for shorter links, at data rates of 10-Gb/s and above.

Architecture

This transceiver system is designed for non-return to zero (NRZ) data communication over more than 2 km of SMF. It consists of two parallel high-speed optoelectronic transceivers, each running at 10-Gb/s, integrated together on the same die. The complete architecture of the system is shown in Fig. 1. Each channel consists of a transmit (TX) and a receive (RX) path.

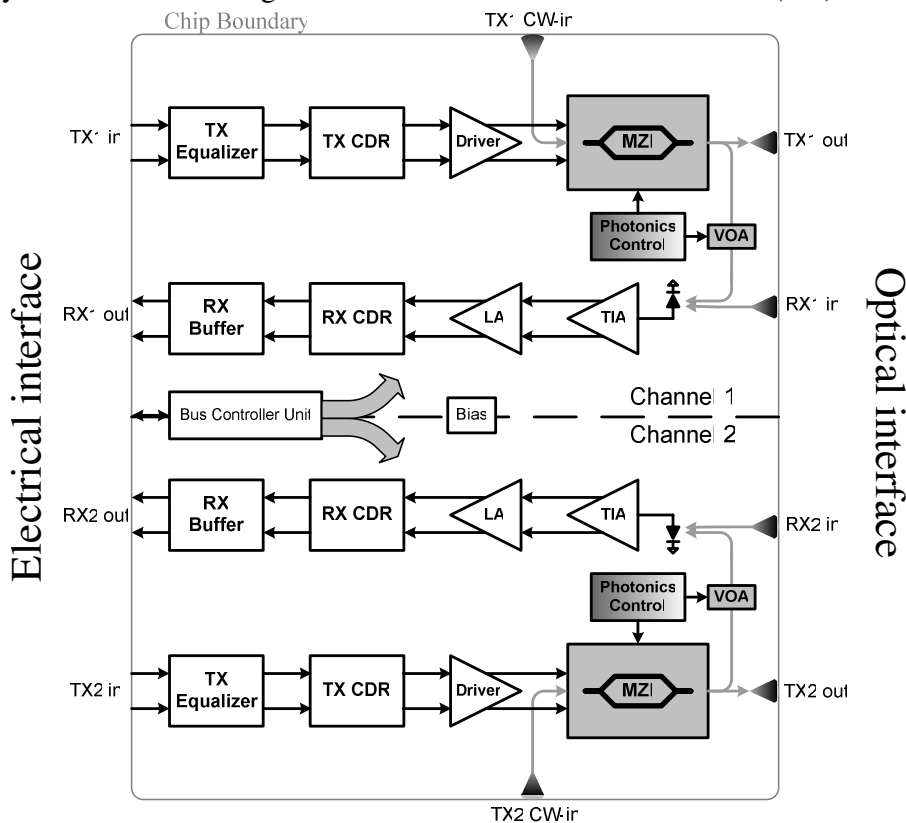


Fig. 1: Dual channel 10Gb/s per channel optoelectronic transceiver architecture.

Experimental Results

The two channel transceiver supports an aggregate data rate in excess of 20 Gb/s. The complete system level performance is summarized in Table 1.

Die Size	8mm x 5.6mm
Wavelength	1535-1555nm
Link Reach	>2000m
Channel Data Rate Range	9.5-11Gb/s
Chip Power Consumption (Total for two channels)	2.5W

Table 1: System performance summary

Section V – Conclusion

A complete 20-Gb/s optical transceiver system has been demonstrated, integrating key optical and electrical components on a single substrate using a 0.13 μm CMOS SOI process.

References

- [1] J.W. Goodman, F.J. Leonberger, S.-Y. Kung, and R.A. Athale, "Optical interconnections for VLSI systems," *Proc. of the IEEE*, vol. 72, pp.850-866, July 1984.
- [2] D.A.B. Miller, "Rationale and challenges for optical interconnects to electronics chips," *Proc. of the IEEE*, vol.88, pp.728-749, June 2000.
- [3] S. Bates and K. Iniewski, "10 GBPS over copper lines - state of the art in VLSI," *Proc. Fifth International Workshop on System-on-Chip for Real-Time Applications*, pp.491-494, July 2005.
- [4] T. Beukema et al., "A 6.4-Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2633-2645, Dec. 2005.